Electronic Version
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Claims

[c1] What is claimed is:

1.An electrostatic discharge (ESD) protection MOS device, comprising:

a silicon substrate of first conductivity type;

an epitaxial silicon layer of said first conductivity type grown on said silicon substrate;

a first ion well of said first conductivity type disposed in said epitaxial silicon layer;

a second ion well of said second conductivity type disposed in said epitaxial silicon layer, said second ion well encompassing said first ion well and laterally isolating said first ion well;

a buried layer of said second conductivity type disposed at interface between said silicon substrate and said epitaxial silicon layer, wherein said buried layer borders said second ion well, thereby fully isolating said first ion well;

a first isolation structure consisting of a gate insulating layer and a field oxide layer, wherein said first isolation structure is formed on said epitaxial silicon layer between said first and second ion wells;

a gate laid over said gate insulating layer and field oxide

layer;

a second isolation structure spaced apart from said first isolation structure, said second isolation structure being formed on said second ion well;

a source doping region of said second conductivity type disposed in said first ion well between said gate insulating layer and said second isolation structure; and

a drain doping region of said second conductivity type disposed in said second ion well between said field oxide layer and said second isolation structure.

[c2] 2.The ESD protection MOS device according to claim 1 wherein said first conductivity type is P type and said second conductivity type is N type.

[c3] 3.The ESD protection MOS device according to claim 1 further comprising a heavily doping region of said first conductivity type disposed in said first ion well between said gate insulating layer and said second isolation structure, wherein said heavily doping region of said first conductivity type and said source doping region of said second conductivity type are shorted together to the same voltage level.

[c4] 4.The ESD protection MOS device according to claim 1 further comprising a field ion well of said first conductivity type adjacent to said second ion well, wherein said

field ion well is located directly under said second isolation structure.

[c5] 5.The ESD protection MOS device according to claim 1 wherein said buried layer of said second conductivity type is formed by ion implanting antimony (Sb) into said silicon substrate at an implant dose of at least 1E15 atoms/cm^2 and at an implant energy of about 80KeV.

[c6] 6.The ESD protection MOS device according to claim 1 wherein said buried layer of said second conductivity type is formed by ion implanting antimony (Sb) into said silicon substrate at an implant dose of about 2E15 atoms/cm^2 and at an implant energy of about 80KeV.

[c7] 7.The ESD protection MOS device according to claim 1 having a channel width to length ratio (W/L) of about 20/3.

[c8] 8.An integrated circuit chip comprising at least one I/O pin, internal circuit, and an NMOS device having protection against electrostatic discharge, said NMOS device comprising:

a P type silicon substrate;

a P type epitaxial silicon layer grown on said silicon substrate;

a P type first ion well disposed in said epitaxial silicon

layer;

a N type second ion well disposed in said epitaxial silicon layer, said second ion well encompassing said first ion well and laterally isolating said first ion well;

a N type buried layer disposed underneath said first ion well, wherein said buried layer borders said second ion well, thereby fully isolating said first ion well from said silicon substrate;

a first isolation structure consisting of a gate insulating layer and a field oxide layer, wherein said first isolation structure is formed on said epitaxial silicon layer between said first and second ion wells;

a gate laid over said gate insulating layer and field oxide layer;

a second isolation structure spaced apart from said first isolation structure, wherein said second isolation structure is substantially formed on said second ion well;

an N type source doping region disposed in said first ion well between said gate insulating layer and said second isolation structure; and

an N type drain doping region disposed in said second ion well between said field oxide layer and said second isolation structure;

wherein said internal circuit of said integrated circuit chip comprises a high-voltage (HV) NMOS device having the same structure as said NMOS device except that said

HV NMOS device does not have said N type buried layer.

[c9] 9.The integrated circuit chip according to claim 8 wherein said NMOS device further comprises a P type heavily doping region disposed in said first ion well between said gate insulating layer and said second isolation structure, wherein said P type heavily doping region and said N type source doping region are shorted together to the same voltage level.

[c10] 10.The integrated circuit chip according to claim 9 wherein said voltage level is V_{SS}.

[c11] 11.The integrated circuit chip according to claim 8 wherein said N type drain doping region of said NMOS device is biased to said I/O pin.

[c12] 12The integrated circuit chip according to claim 8 wherein said gate of said NMOS device is coupled to said N type source doping region.

[c13] 13.The integrated circuit chip according to claim 8 wherein said NMOS device further comprises a P type field ion well adjacent to said second ion well, wherein said P type field ion well is located directly under said second isolation structure.

[c14] 14.The integrated circuit chip according to claim 8

wherein said N type buried layer is formed by ion implanting antimony (Sb) into said silicon substrate at an implant dose of at least 1E15 atoms/cm^2 and at an implant energy of about 80KeV.

[c15] 15.The integrated circuit chip according to claim 8 wherein said N type buried layer is formed by ion implanting antimony (Sb) into said silicon substrate at an implant dose of about 2E15 atoms/cm^2 and at an implant energy of about 80KeV.

[c16] 16.The integrated circuit chip according to claim 8 wherein said NMOS device has a channel width to length ratio (W/L) of about 20/3.

[c17] 17.The integrated circuit chip according to claim 8 wherein said HV NMOS device is a 40V HV NMOS device.

[c18] 18.An integrated circuit chip comprising at least one I/O pin, internal circuit, and an NMOS device having protection against electrostatic discharge, said NMOS device comprising:

a P type silicon substrate;

a P type epitaxial silicon layer grown on said silicon substrate;

a P type first ion well disposed in said epitaxial silicon layer;

a N type second ion well disposed in said epitaxial silicon layer, said second ion well encompassing said first ion well and laterally isolating said first ion well;

a N type buried layer disposed underneath said first ion well, wherein said buried layer borders said second ion well, thereby fully isolating said first ion well from said silicon substrate;

a first isolation structure consisting of a gate insulating layer and a field oxide layer, wherein said first isolation structure is formed on said epitaxial silicon layer between said first and second ion wells;

a gate laid over said gate insulating layer and field oxide layer;

a second isolation structure spaced apart from said first isolation structure, wherein said second isolation structure is substantially formed on said second ion well;

an N type source doping region disposed in said first ion well between said gate insulating layer and said second isolation structure; and

an N type drain doping region disposed in said second ion well between said field oxide layer and said second isolation structure;

wherein said internal circuit of said integrated circuit chip comprises a high-voltage (HV) NMOS device having the same structure as said NMOS device except that said HV NMOS device has a buried diffusion layer with a dop-

ing concentration that is smaller than that of said N type buried layer of said NMOS device.

[c19] 19.The integrated circuit chip according to claim 18 wherein said NMOS device further comprises a P type heavily doping region disposed in said first ion well between said gate insulating layer and said second isolation structure, wherein said P type heavily doping region and said N type source doping region are shorted together to the same voltage level.

[c20] 20.The integrated circuit chip according to claim 19 wherein said voltage level is V_{SS}.

[c21] 21.The integrated circuit chip according to claim 18 wherein said N type drain doping region of said NMOS device is biased to said I/O pin.

[c22] 22.The integrated circuit chip according to claim 18 wherein said gate of said NMOS device is coupled to said N type source doping region.

[c23] 23.The integrated circuit chip according to claim 18 wherein said N type buried layer is formed by ion implanting antimony (Sb) into said silicon substrate at an implant dose of at least 1E15 atoms/cm^2 and at an implant energy of about 80KeV.

[c24] 24.The integrated circuit chip according to claim 18 wherein said NMOS device has a channel width to length ratio (W/L) of about 20/3.

[c25] 25.The integrated circuit chip according to claim 18 wherein said HV NMOS device is a 40V HV NMOS device.